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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/651,522	08/29/2003	Kenji Masumoto	TI-35484	8862

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EXAMINER	
ROMAN, ANGEL	
ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/651,522	MASUMOTO, KENJI	
	Examiner	Art Unit	
	Angel Roman	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *19 and 20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 12-17* is/are rejected.

7)☒ Claim(s) *11 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-18, drawn to a semiconductor device, classified in class 257, subclass 782.

   II. Claims 19 and 20, drawn to a method of making a semiconductor device, classified in class 438, subclass 118.

2. The inventions are distinct, each from the other because of the following reasons: Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case instead of disposing the polymeric material on the interposer surface the polymeric material could be disposed on the semiconductor chip back surface.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with Wade Brady on 01/31/05 a provisional election was made with traverse to prosecute the invention of Group I, claims 1-18. Affirmation of this election must be made by applicant in replying to this Office action. Claims 19 and 20 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

5. It is suggested that Applicant cancel non-elected claims 19 and 20 in response to this office action.

Oath/Declaration

The Oath documents submitted on 12/12/03 are acceptable.

Drawings

6. The formal Drawings filed 12/12/03 are acceptable.

Specification

7. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: PACKAGE FOR SEMICONDUCTOR DEVICE HAVING A DEVICE-SUPPORTING POLYMERIC MATERIAL COVERING A SOLDER BALL ARRAY AREA

Claim Objections

8. Claim 1 is objected to because of the following informalities: In line 9, "the area", should be replaced with –an area–. Appropriate correction is required.

9. Claim 15 is objected to because of the following informalities: In line 7, "the area", should be replaced with --an area--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 1-10 13 and 14 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Amagai et al. U.S. Patent 6,232,661 B1.

Regarding claim 1, Amagai et al. discloses a semiconductor device 1 comprising; an interposer 3 having two major surfaces wherein the first surface includes patterned metal conductors and bond pads and the second surface includes an array of solder balls 7 (see figure 3); a semiconductor chip 2 having a top surface and a back surface, said back surface of said chip 2 adjacent said interposer 3, and said top surface comprising a plurality of terminals (see figure 3); a layer of polymeric material 8 disposed on said first surface of the interposer 3 covering an area of the interposer 3 over the array of solder balls 7, at least a portion of said polymeric material 8 between

said chip 2 and said interposer 3 (see figure 3); a plurality of electrical connections 5 between said chip terminals and said bond pads on the interposer 3 (see column 5, lines 35-40).

Regarding claim 2, Amagai et al. discloses an area of the chip 2 being smaller than the area of the solder ball array (see figure 3).

Regarding claims 3, Amagai et al. discloses the interposer comprising a flexible film (see column 5, lines 13-15).

Regarding claims 4, Amagai et al. discloses the interposer 3 comprising a thin laminate (see column 5, lines 13-15).

Regarding claims 5, Amagai et al. discloses the interposer 3 comprising a thin composite material (see column 5, lines 13-20).

Regarding claim 6, Amagai et al. discloses the elastic modulus of said layer of polymeric material 8 in a range of about 1-15 Gpa (see column 6, lines 37-45).

Regarding claim 7, Amagai et al. discloses the thickness of said layer of polymeric material 8 in a range of about 75 to about 200 microns (see column 6, lines 21-22).

Regarding claim 8, Amagai et al. discloses the polymeric material being thermally conductive (see column 5, lines 56-60).

Regarding claim 9, Amagai et al. discloses the polymeric material 8, comprising a thermosetting paste (see column 5, lines 56-60).

Regarding claim 10, Amagai et al. discloses the polymeric material 8 being a preformed film (see column 5, lines 56-60).

Regarding claim 13, Amagai et al. discloses the solder balls 7 being in a fully populated array on the interposer 3 (see figure 3).

Regarding claim 14, Amagai et al. discloses positioning the edges of the chip 2 over one or more of the solder balls 7 (see figure 3).

12. Claim 15 is rejected under 35 U.S.C. 102(b) as being anticipated by Dudderar et al. U.S. Patent 6,020,219 A.

Dudderar et al. discloses a semiconductor device comprising; an interposer 200 having first and second major surfaces, wherein said first major surface includes patterned metal conductors and bond pads (262, 266) and the second major surface includes an array of solder balls (201, 202, 203, 204) connected to selected pads on the

first surface; a semiconductor chip 300 comprising top and back surfaces and having an area smaller than an area of said solder ball array, said back surface of said chip 300 adhered to said major surface of said interposer 200, and said top surface of said chip 300 including a plurality of terminals (301, 302) located on a top surface (see figure 1); a plurality of polymeric structures 252 (see column 4, lines 47-50 and column 5, lines 15-25) disposed on said firs major surface of the interposer 200, each of said polymeric structures 252 over a solder ball location in said array of solder balls (201, 202, 203, 204); and a plurality of electrical connections (311, 312) between said chip terminals (301, 302) and said bond pads (262, 266) on the interposer 200 (see figure 1).

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

15. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Amagai et al. U.S. Patent 6,232,661 B1 in view of Yamamoto et al. U.S. Patent 6,265,782 B1.

Amagai et al. is applied as above but lacks anticipation on disclosing gold as a material used for the electrical connections. Yamamoto et al. discloses using gold wires for electrically connecting a device to a substrate (see column 21, lines 53-56); in view of this disclosure, it would have been obvious to a person having ordinary skills in the art at the time the invention was made to use gold wires as disclosed in Yamamoto et al. for the electrical connection in the primary reference of Amagai et al. in order to obtain a desire conductivity. Furthermore the particular type of material used to make the wires is only considered to be the use of a " preferred " or " optimum " material out of a plurality of well known materials that a person having ordinary skill in the art at the time the invention was made would have find obvious to provide using routine experimentation.

16. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dudderar et al. U.S. Patent 6,020,219 A in view of Amagai et al. U.S. Patent 6,232,661 B1.

Dudderar et al. is applied as above but lacks anticipation on disclosing an elastic modulus of said layer of polymeric material in a range of about 1-15 Gpa and a thickness of said layer of polymeric material in a range of about 75 to about 200 microns. Amagai et al. discloses an elastic modulus of a layer of polymeric material in a range of about 1-15 Gpa and a thickness of said layer of polymeric material in a range

of about 75 to about 200 microns (see column 6, lines 21-45), in view of this disclosure, it would have been obvious to a person having ordinary skills in the art at the time the invention was made to use a polymeric material disclosed in Amagai et al. in the primary reference of Dudderar et al. in order to prevent damage to the semiconductor device.

Allowable Subject Matter

17. Claims 11 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

18. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record either singularly or in combination failed to anticipate or render obvious the limitations of disclosing a polymeric material comprising an insulator and a metal-filled polymer as required by claim 11 and disclosing the polymeric structures preformed on a dielectric film as required by claim 18.

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Aoki et al., DiStefano, Fujisawa et al. and Igarashi et al. disclose semiconductor devices having polymeric materials interposed between substrates and devices, the polymeric materials covering ball grid array areas on the substrate.

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel Roman whose telephone number is (571) 272-1681. The examiner can normally be reached on Monday-Friday 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AR
February 22, 2005

MICHAEL S. LEBENTRITT
PRIMARY EXAMINER